

ECE212/212s Lecture Notes

Lecture: Chapter 7

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Register

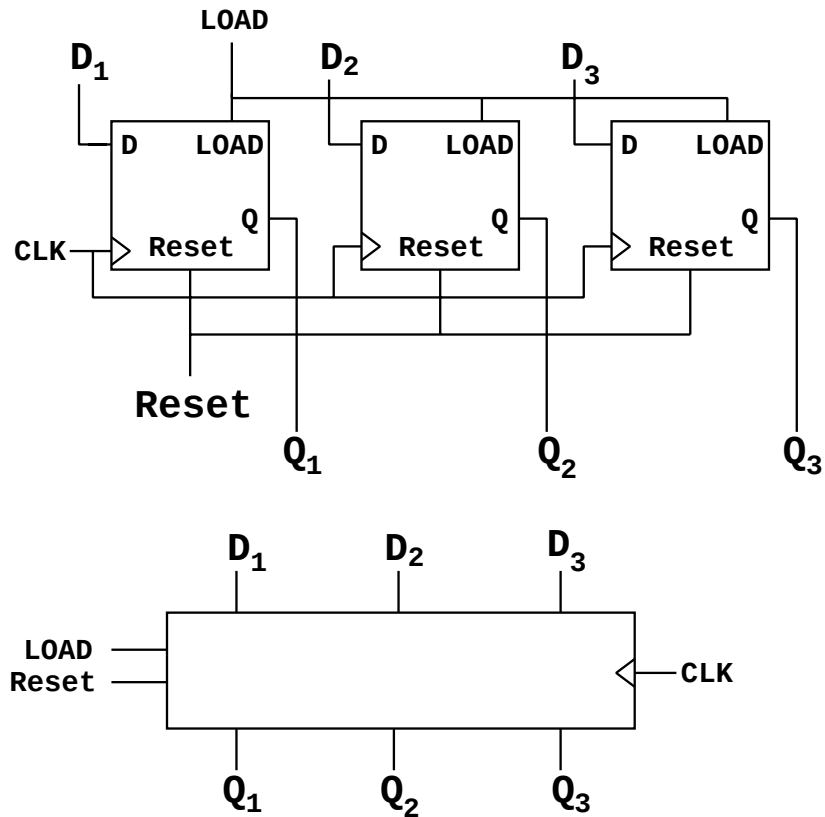


Figure 1: A loadable 3-bit register

TTL 74374 and 74377 Octal D-type FFs (Registers) with enable

$$OE = 0 \quad Q_i = Z$$

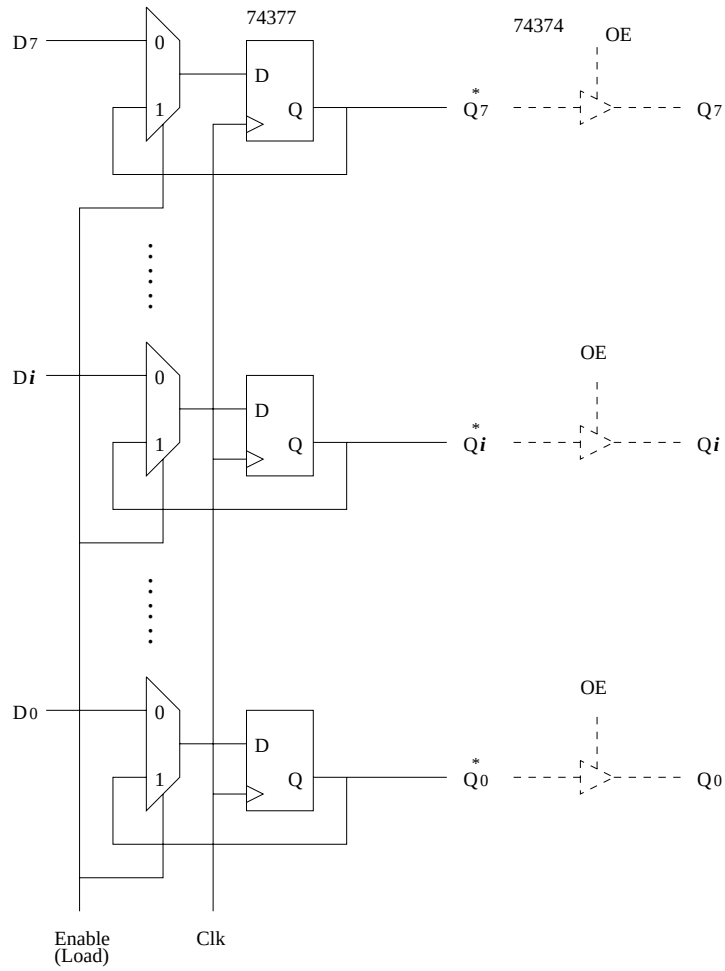
$$OE = 1 \quad Q_i = Q_i^*$$

Truth Table for 74374

$\overline{OE}$	CLK	D	Q
1	x	x	z
0	$\uparrow$	0	0
0	$\uparrow$	1	1
0	$\downarrow$	x	-

Truth Table for 74377

$\overline{EN}$	CLK	D	Q
1	x	x	-
0	$\uparrow$	0	0
0	$\uparrow$	1	1
0	$\downarrow$	x	-



Shift Register (3-bit)

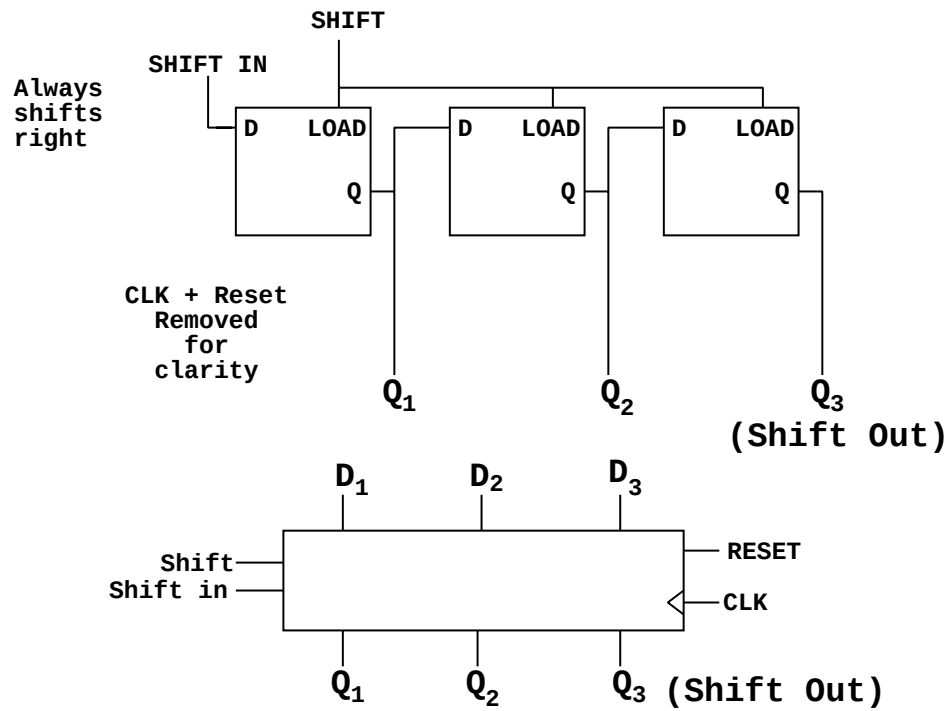


Figure 2: A 3-bit shift register (Always shifts right)

Note: Clock and Reset signals are removed for clarity.

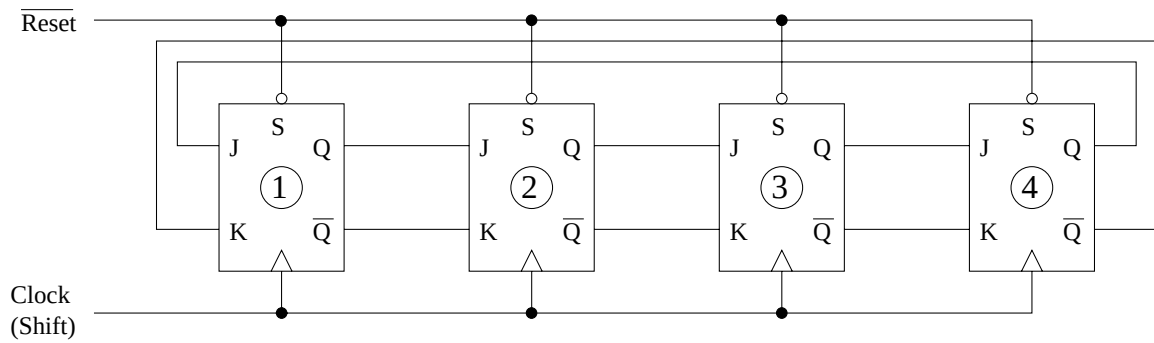
Circular Shift Register with JK FF's

Shift Right → Multiply by 2

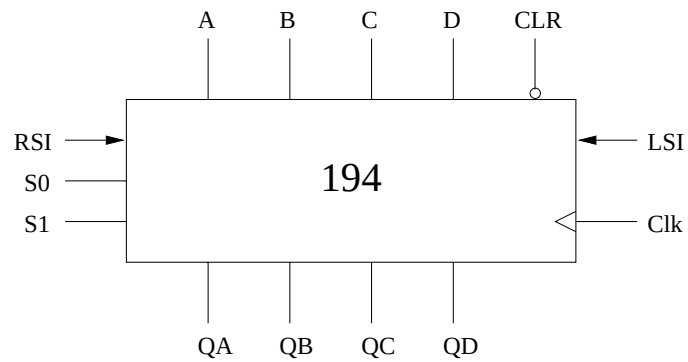
Shift Left → Divide by 2

74194 4-bit Bidirectional Universal Shift Register

CLR	S0	S1	Clk	QA	QB	QC	QD	Description
0	X	X	X	0	0	0	0	
1	1	1	↑	A	B	C	D	(LOAD)
1	0	1	↑	RSI	QA	QB	QC	(Shift right)
1	1	0	↑	QB	QC	QD	LSI	(Shift left)
1	0	0	X	QA	QB	QC	QD	(HOLD)



Reset	Q1	Q2	Q3	Q4	
0	1	0	0	0	8
1	0	1	0	0	4
1	0	0	1	0	2
1	0	0	0	1	1



CLR is asynchronous

(See page 333)

Register Files & RAM's

RAM - Random Access Memory: A collection of registers, each with a unique address (address decode logic). TTL 74670 4×4 register file (RAM). Contains 4, 4-bit registers (16 D-FF's).

$R/\overline{W} = 1$ (Enable Read)

$R/\overline{W} = 0$ (Enable Write)

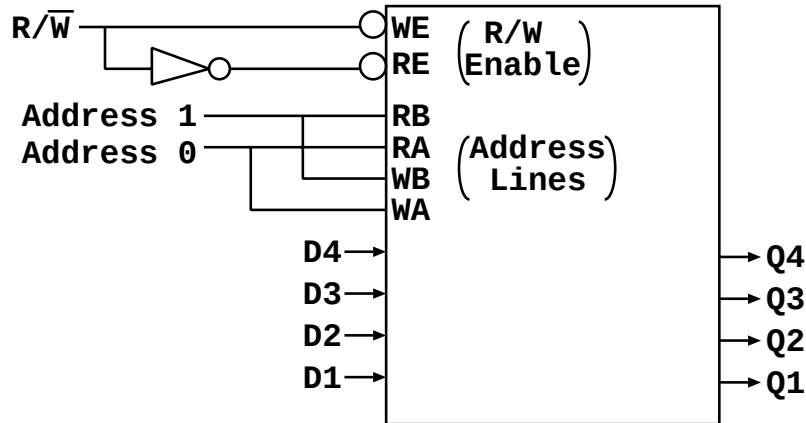
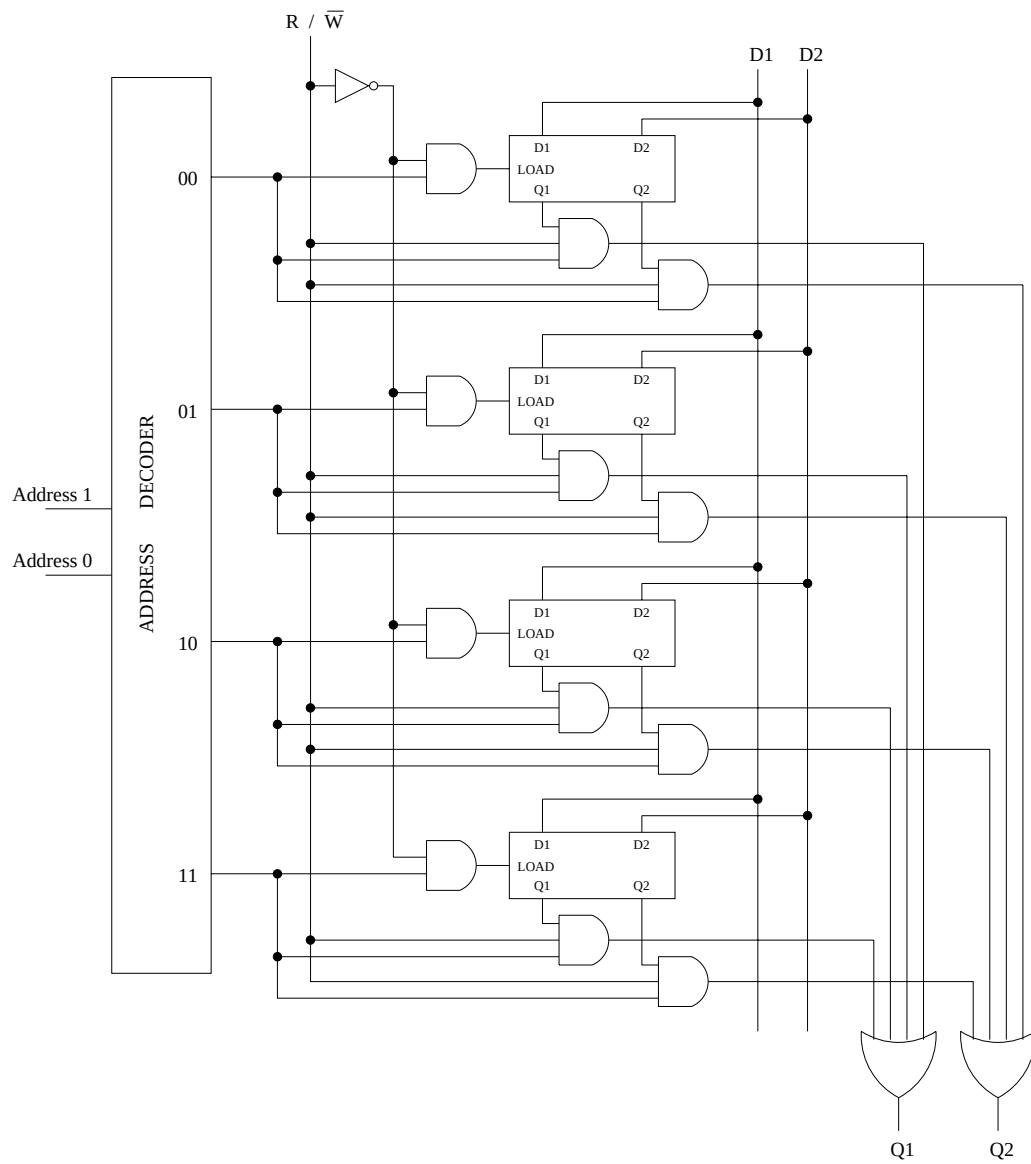


Figure 3: Unlocked Memory

$R/\overline{W}$	Address 1	Address 0	D4	D3	D2	D1	Q4	Q3	Q2	Q1	Description
0	0	0	1	1	0	0	X	X	X	X	Write 12 to address 0
0	1	0	1	0	1	0	X	X	X	X	Write 10 to address 0
1	0	0	X	X	X	X	1	1	0	0	Read data at address 0
1	1	0	X	X	X	X	1	0	1	0	Read data at address 2

A 4 x 2 Memory



Address	Data
00	10
01	01
10	11
11	11

(Data is stored prior to use)

Read (Enable)	Address 1	Address 0	Q2	Q1	Description
1	1	0	0	1	Read at address 2
1	0	0	1	1	Read at address 0

Counters

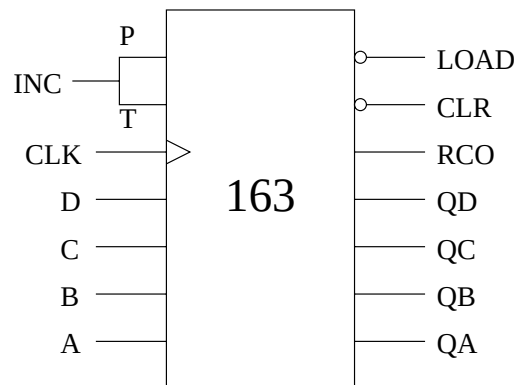
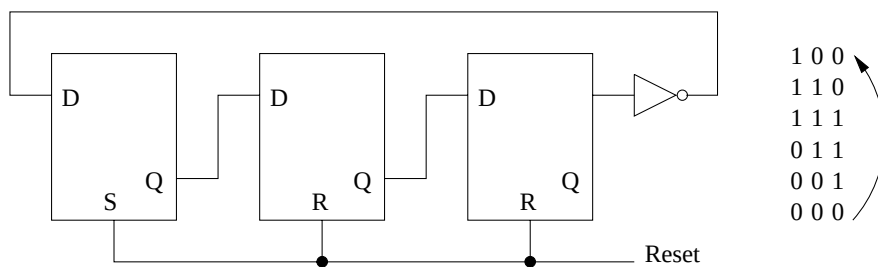
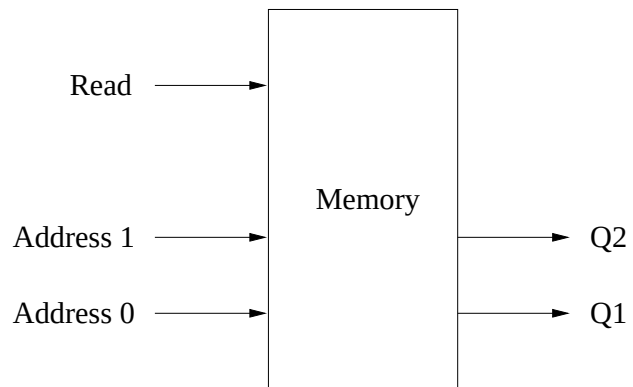
- Up Counters (count up)
- Down Counters (count down)
- Up/Down Counters (count up + down)
- Loadable Counters
- Decade counters (BCD counters $1 \dots \rightarrow \dots 9$)
- Grey Code (0000, 0001, 0011, 0010, 0110, 0111, ...)
(KMAP concept) (0, 1, 3, 2, 6, 7, ...)
- Ring Counters (Circular Shift Register)

Johnson Counter

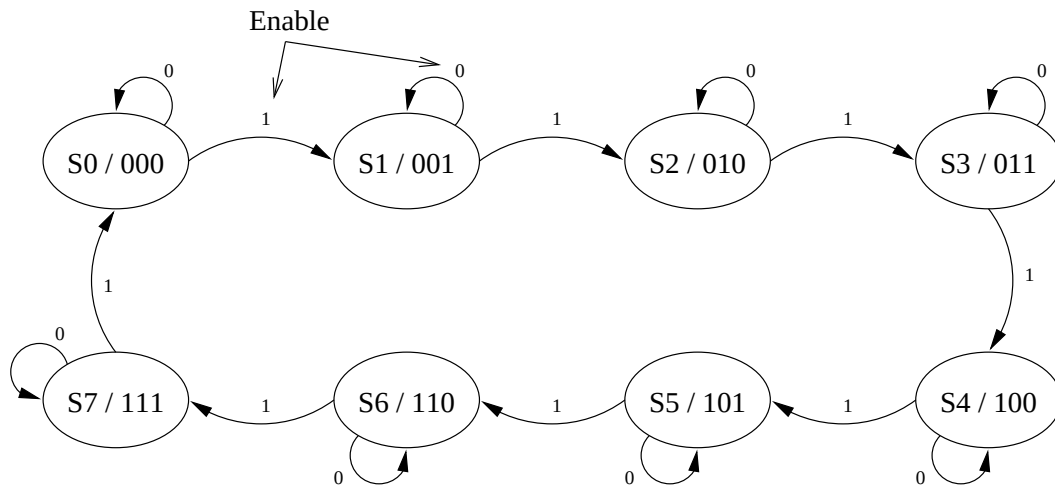
74163 4-bit Up Counter

CLR	LOAD	P	T	QA	QB	QC	QD	Description
0	1	X	X	0	0	0	0	CLEAR
1	0	X	X	A	B	C	D	LOAD
1	1	0	0	QA	QB	QC	QD	HOLD
1	1	1	1	-	-	-	-	COUNT UP

What is RC0 for?



3-bit Up Counter with Enable

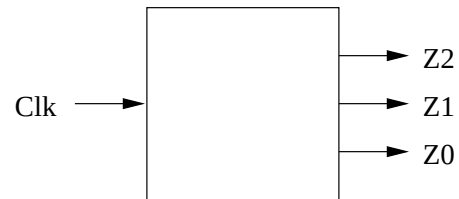


STT Symbolic

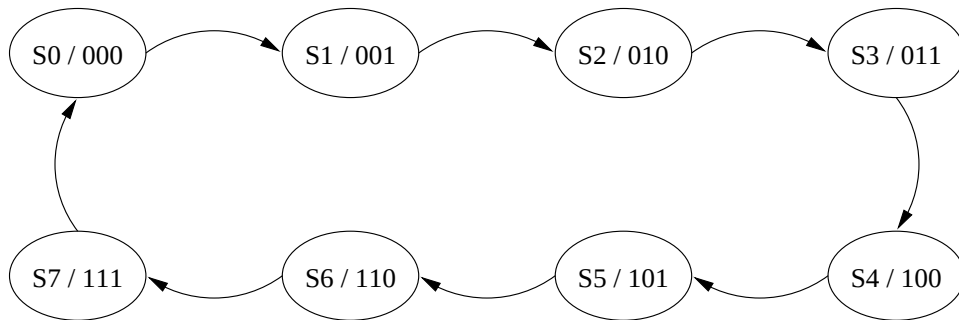
PS	NS				
	Enable = 0	Enable = 1	Z_2	Z_1	Z_0
S_0	S_0	S_1	0	0	0
S_1	S_1	S_2	0	0	1
S_2	S_2	S_3	0	1	0
S_3	S_3	S_4	0	1	1
S_4	S_4	S_5	1	0	0
S_5	S_5	S_6	1	0	1
S_6	S_6	S_7	1	1	0
S_7	S_7	S_0	1	1	1

A 3-bit up-counter (using T FF's)

Block diagram



State Diagram (Moore Machine)



Note: No inputs, Clock Signals transitions.

	PS	NS	OUTPUT			
			Z_1	Z_2	Z_3	
<u>STT (Symbolic)</u>	S0	S1	0	0	0	$S_0 \Rightarrow 000$
	S1	S2	0	0	1	$S_1 \Rightarrow 001$
	S2	S3	0	1	0	$S_2 \Rightarrow 010$
	S3	S4	0	1	1	$S_3 \Rightarrow 011$
	S4	S5	1	0	0	$S_4 \Rightarrow 100$
	S5	S6	1	0	1	$S_5 \Rightarrow 101$
	S6	S7	1	1	0	$S_6 \Rightarrow 110$
	S7	S0	1	1	1	$S_7 \Rightarrow 111$

State Assignment

Excitation table for T Flip-flop.

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

STT Encoded

PS			NS			OUTPUT		
Y_2	Y_1	Y_0	Y_2^+	Y_1^+	Y_0^+	Z_1	Z_2	Z_3
0	0	0	0	0	1	0	0	0
0	0	1	0	1	0	0	0	1
0	1	0	0	1	1	0	1	0
0	1	1	1	0	0	0	1	1
1	0	0	1	0	1	1	0	0
1	0	1	1	1	0	1	0	1
1	1	0	1	1	1	1	1	0
1	1	1	0	0	0	1	1	1

PS			NS			OUTPUT		
Y_2	Y_1	Y_0	$T_{Y_2}^+$	$T_{Y_1}^+$	$T_{Y_0}^+$	Z_1	Z_2	Z_3
0	0	0	0	0	1	0	0	0
0	0	1	0	1	1	0	0	1
0	1	0	0	0	1	0	1	0
0	1	1	1	1	1	0	1	1
1	0	0	0	0	1	1	0	0
1	0	1	0	1	1	1	0	1
1	1	0	0	0	1	1	1	0
1	1	1	1	1	1	1	1	1

$Y_2 Y_1$					
Y_0	0	0	0	0	0
	1	0	1	1	0

$$TY_2^+ = Y_1 Y_0$$

$Y_2 Y_1$					
Y_0	0	0	0	0	0
	1	1	1	1	1

$$TY_1^+ = Y_0$$

$Y_2 Y_1$					
Y_0	0	1	1	1	1
	1	1	1	1	1

$$TY_0^+ = 1$$

$$Z_2 = Y_2$$

$$Z_1 = Y_1$$

$$Z_0 = Y_0$$

Self Starting Counters

Every possible state leads to a desired count sequence.

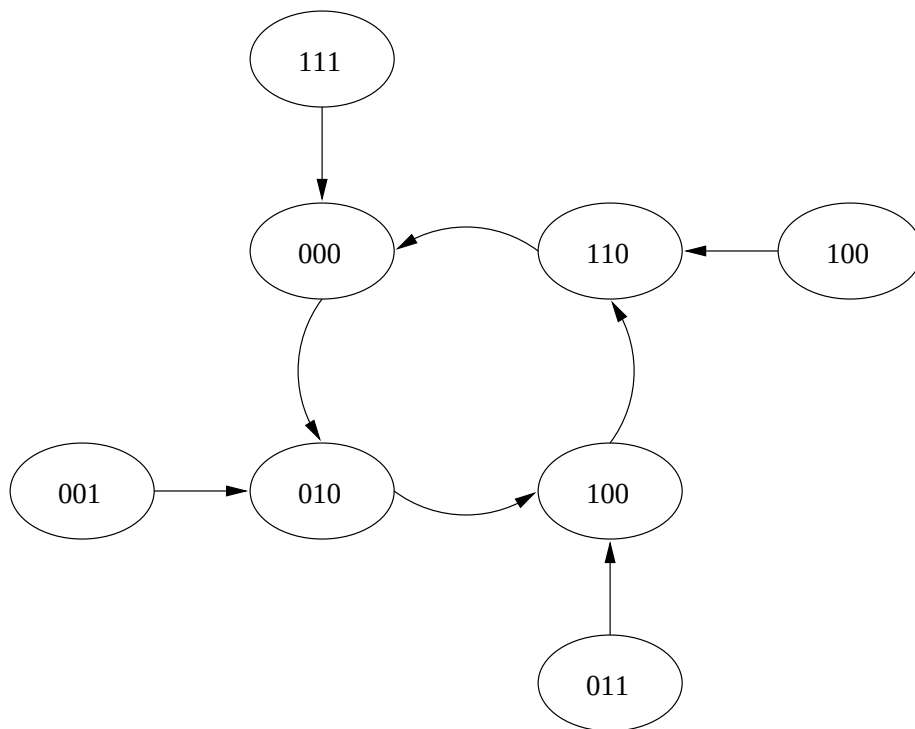
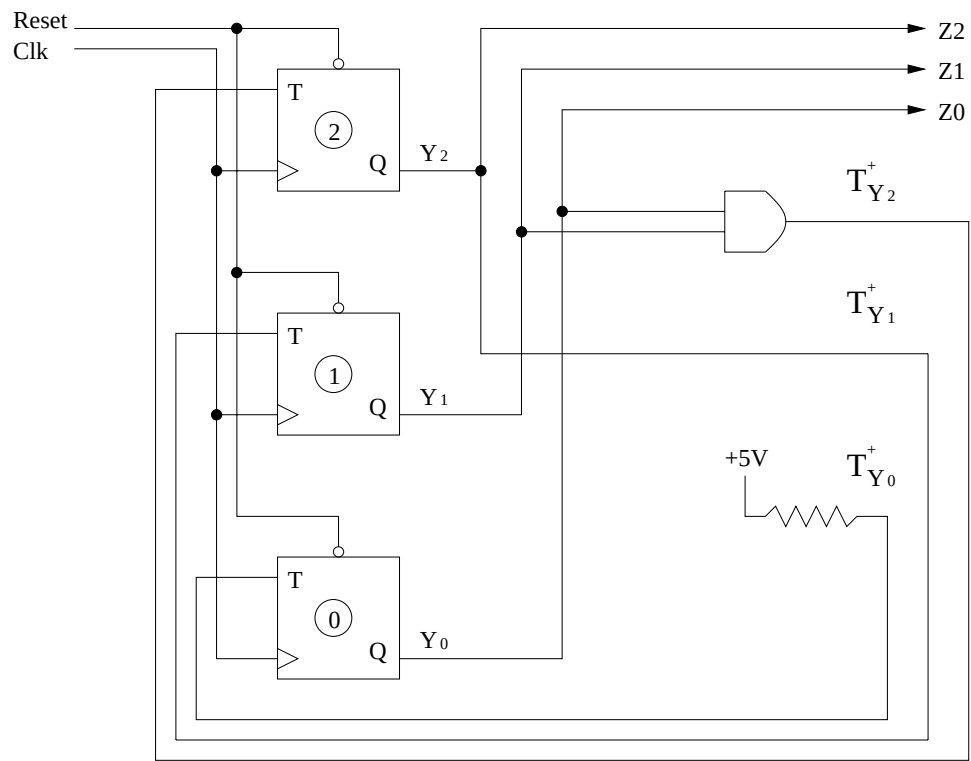


Figure 4: This counter is self-starting

Example A: Design a 4-bit BCD up counter.

Solution 1:

A four-bit BCD up counter

Solution 2:

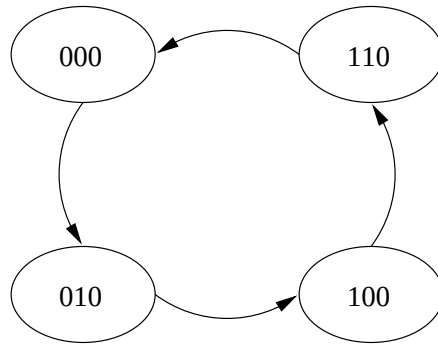


Figure 5: this counter is not self-starting

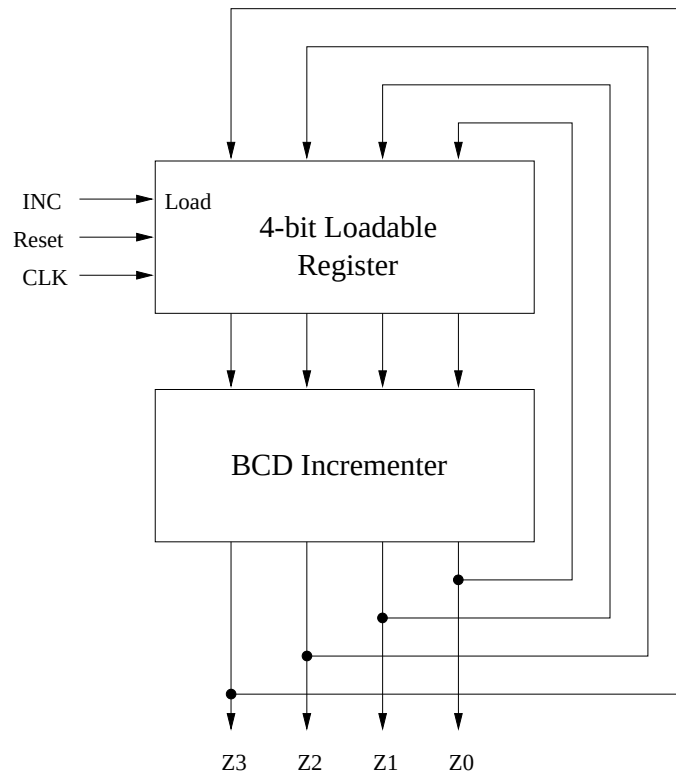


Figure 6: A 4-bit BCD up counter (Brute Force Method)

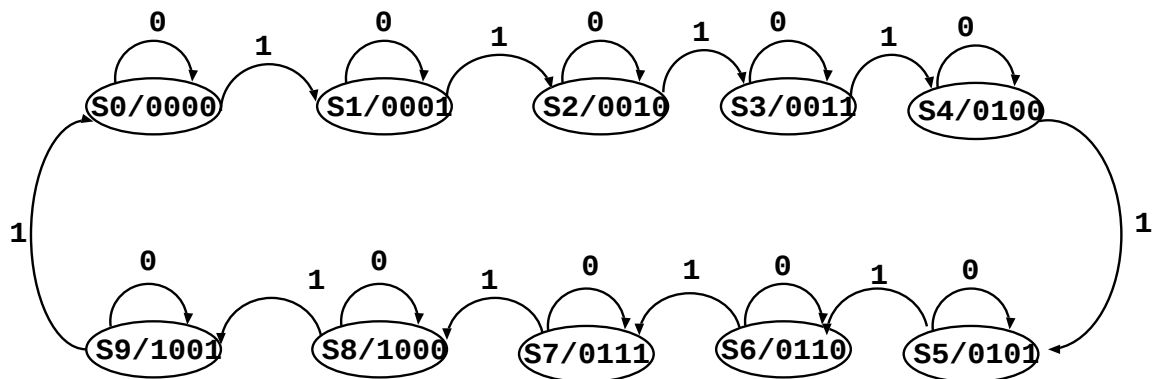


Figure 7: (General Method) Inputs: INC

State Table (Symbolic)

Input	PS	NS	Output			
INC			Z_3	Z_2	Z_1	Z_0
0	S0	S0	0	0	0	0
1	S0	S1	0	0	0	0
0	S1	S1	0	0	0	1
1	S1	S2	0	0	0	1
0	S2	S2	0	0	1	0
1	S2	S3	0	0	1	0
0	S3	S3	0	0	1	1
1	S3	S4	0	0	1	1
0	S4	S4	0	1	0	0
1	S4	S5	0	1	0	0
0	S5	S5	0	1	0	1
1	S5	S6	0	1	0	1
0	S6	S6	0	1	1	0
1	S6	S7	0	1	1	0
0	S7	S7	0	1	1	1
1	S7	S8	0	1	1	1
0	S8	S8	1	0	0	0
1	S8	S9	1	0	0	0
0	S9	S9	1	0	0	1
1	S9	S0	1	0	0	1

State Assignment

$S_0 \Rightarrow 0000$
 $S_1 \Rightarrow 0001$
 $S_2 \Rightarrow 0010$
 $S_3 \Rightarrow 0011$
 $S_4 \Rightarrow 0100$
 $S_5 \Rightarrow 0101$
 $S_6 \Rightarrow 0110$
 $S_7 \Rightarrow 0111$
 $S_8 \Rightarrow 1000$
 $S_9 \Rightarrow 1001$

STT (Encoded)

INC	PS				NS				OUTPUT			
	Y_3	Y_2	Y_1	Y_0	Y_3^+	Y_2^+	Y_1^+	Y_0^+	Z_3	Z_2	Z_1	Z_0
0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	1	0	0	0	1	0	0	0	1
1	0	0	0	1	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	1	0	0	0	1	0
1	0	0	1	0	0	0	1	1	0	0	1	0
0	0	0	1	1	0	0	1	1	0	0	1	1
1	0	0	1	1	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	0	0	0	1	0	0
1	0	1	0	0	0	1	0	1	0	1	0	0
0	0	1	0	1	0	1	0	1	0	1	0	1
1	0	1	0	1	0	1	1	0	0	1	0	1
0	0	1	1	0	0	1	1	0	0	1	1	0
1	0	1	1	0	0	1	1	1	0	1	1	0
0	0	1	1	1	0	1	1	1	0	1	1	1
1	0	1	1	1	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	0	0	1	0	0	0
1	1	0	0	0	1	0	0	1	1	0	0	0
0	1	0	0	1	1	0	0	1	1	0	0	1
1	1	0	0	1	0	0	0	0	1	0	0	1

INC	PS				NS				OUTPUT			
	Y_3	Y_2	Y_1	Y_0	$D_{Y_3}^+$	$D_{Y_2}^+$	$D_{Y_1}^+$	$D_{Y_0}^+$	Z_3	Z_2	Z_1	Z_0
0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	1	0	0	0	1	0	0	0	1
1	0	0	0	1	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	1	0	0	0	1	0
1	0	0	1	0	0	0	1	1	0	0	1	0
0	0	0	1	1	0	0	1	1	0	0	1	1
1	0	0	1	1	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	0	0	0	1	0	0
1	0	1	0	0	0	1	0	1	0	1	0	0
0	0	1	0	1	0	1	0	1	0	1	0	1
1	0	1	0	1	0	1	1	0	0	1	0	1
0	0	1	1	0	0	1	1	0	0	1	1	0
1	0	1	1	0	0	1	1	1	0	1	1	0
0	0	1	1	1	0	1	1	1	0	1	1	1
1	0	1	1	1	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	0	0	1	0	0	0
1	1	0	0	0	1	0	0	1	1	0	0	0
0	1	0	0	1	1	0	0	1	1	0	0	1
1	1	0	0	1	0	0	0	0	1	0	0	1

Equations after minimizing with Espresso

$$D_{Y_3}^+ = IncY_2Y_1Y_0 + \overline{Inc}Y_3 + Y_3\overline{Y_0}$$

$$D_{Y_2}^+ = Inc\overline{Y_2}Y_1Y_0 + \overline{Inc}Y_2 + Y_2\overline{Y_1} + Y_2\overline{Y_0}$$

$$D_{Y_1}^+ = Inc\overline{Y_3}\overline{Y_1}Y_0 + Y_1\overline{Y_0} + \overline{Inc}Y_1$$

$$D_{Y_0}^+ = Inc\overline{Y_0} + \overline{Inc}Y_0 = Inc \oplus Y_0$$

$$Z_3 = Y_3$$

$$Z_2 = Y_2$$

$$Z_1 = Y_1$$

$$Z_0 = Y_0$$

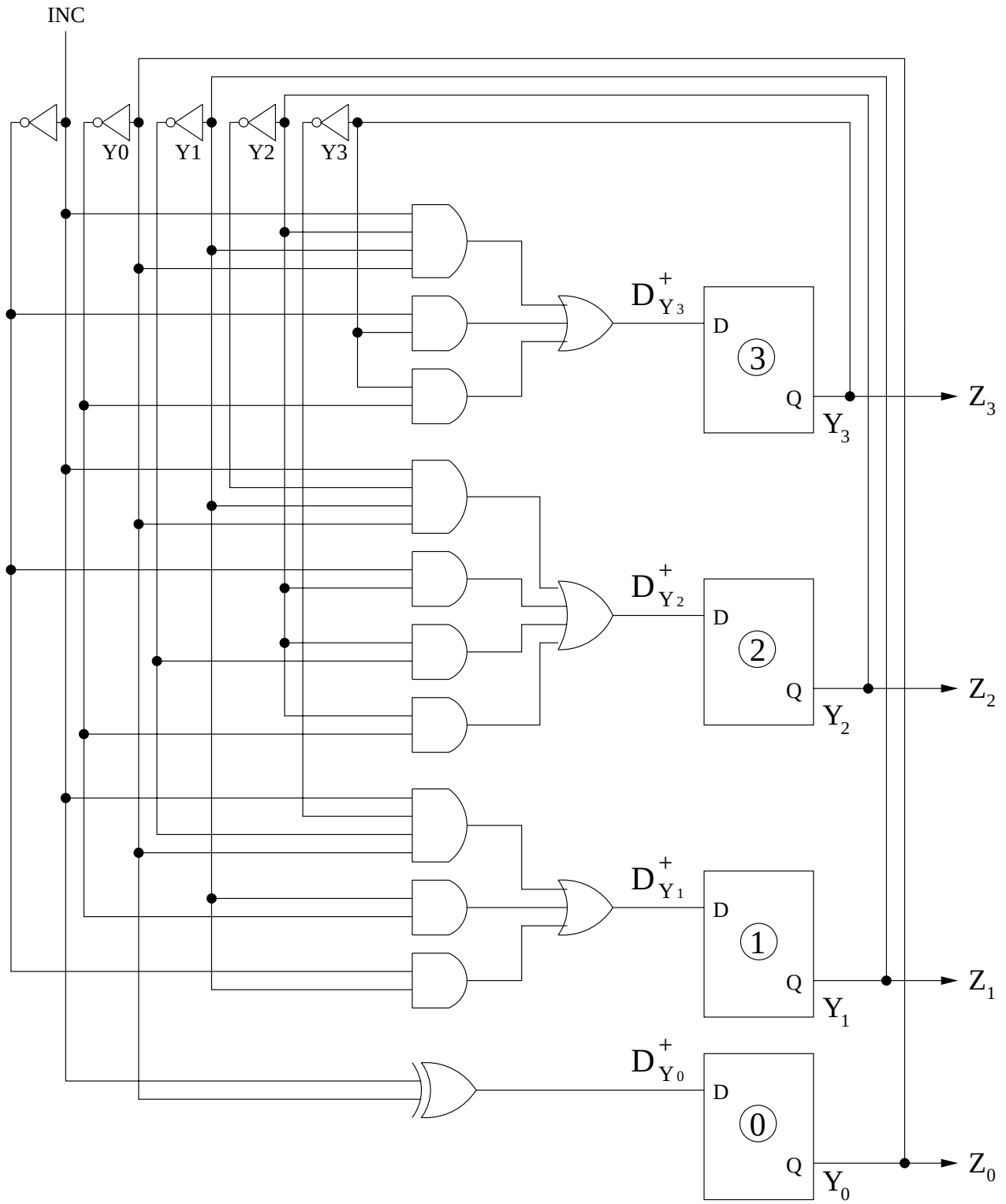


Figure 8: BCD counter schematic