

Question 1	Question 2	Question 3	Question 4	Question 5	Total Points

ECE212 and ECE212s
Fundamentals of Logic Design
Fall 1996
Tuesday, November 12, 1996
Test 2 - Solutions

Name (Please Print)

Social Security Number

This is a 75-minute open-book test. Please put away all papers except the exam itself and your text. You can use the back of the pages for work space. However, make sure that your answers are placed in the space provided for each problem. Clearly indicate your answers. Answer *all* questions and remember to check your answers carefully. Be sure to check the point value of each question before beginning. For partial credit, show your work, especially where the answer is just a number. (b)

Here is a list of questions and subjects.

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1. (*State Reduction - 20 points.*) Given the state table shown below, obtain an equivalent reduced state table containing a minimum number of states using the implication chart method. Make it clear which states have been combined. Also show the reduced state transition table.

PS	NS,Z	
	X=0	X=1
S_0	$S_1, 0$	$S_4, 0$
S_1	$S_2, 0$	$S_1, 0$
S_2	$S_1, 0$	$S_6, 0$
S_3	$S_1, 0$	$S_3, 0$
S_4	$S_5, 0$	$S_4, 0$
S_5	$S_2, 0$	$S_1, 0$
S_6	$S_5, 0$	$S_3, 1$

Solution:

The implication chart for this problem follows.

The implication chart method reveals that $S_0 \equiv S_3$, $S_0 \equiv S_4$, $S_1 \equiv S_5$, and $S_3 \equiv S_4$. This results in two equivalence classes, $\{S_0, S_3, S_4\} \equiv S'_0$ and $\{S_1, S_5\} \equiv S'_1$.

PS	NS,Z	
	X=0	X=1
S'_0	$S'_1, 0$	$S'_0, 0$
S'_1	$S_2, 0$	$S'_1, 0$
S_2	$S'_1, 0$	$S_6, 0$
S_6	$S'_1, 0$	$S'_0, 1$

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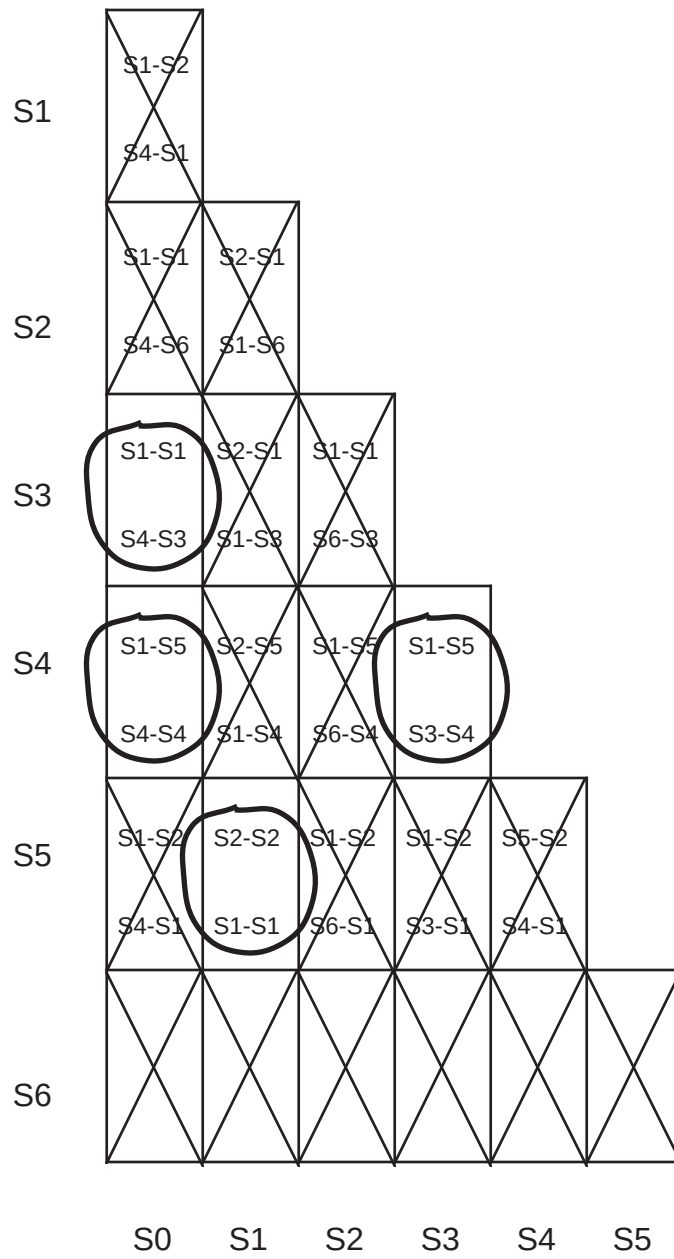


Figure 1: Figure for Problem 1.

2. (*Flip-Flops Conversion - 20 points*) The characteristic equations for a D flip-flop determine that the output Q is updated to either 0 or 1 after each clock cycle. A loadable D flip-flop has one additional input *Load* that allows data to be stored in the flip-flop for more than a single clock cycle. Design a loadable D flip-flop with an active low input *Load* using a normal J-K flip-flop and some combinational logic. Use the characteristic equations for a D flip-flop as a starting point. When the input signal *Load*=0, the flip-flop functions as a normal D flip-flop. When the input signal *Load*=1, the output Q stays at its previous value.

$m_{\#}$	Load	D	Q	Q^+	J	K
0	0	0	0	0	0	X
1	0	0	1	0	X	1
2	0	1	0	1	1	X
3	0	1	1	1	X	0
4	1	0	0	0	0	X
5	1	0	1	1	X	0
6	1	1	0	0	0	X
7	1	1	1	1	X	0

From the table, we find that

$$J = \sum m(2) + \sum d(1, 3, 5, 7) \quad (1)$$

and

$$K = \sum m(1) + \sum d(0, 2, 4, 6) \quad (2)$$

Using a karnaugh map for simplification, we find that

$$J = \overline{Load} D \quad (3)$$

and

$$K = \overline{Load} \overline{D} \quad (4)$$

The circuit implementation for this problem is shown in Figure 2.

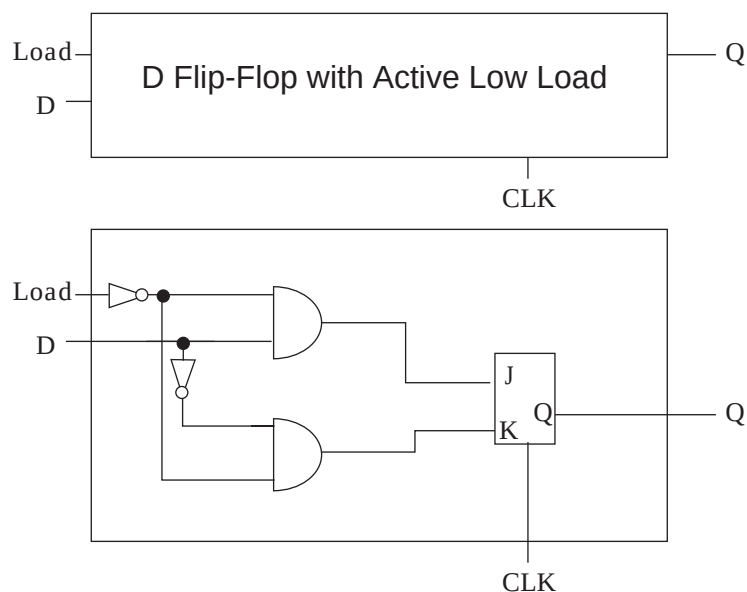


Figure 2: Schematic diagram for Problem 2.

3. (*Finite State Machine/Counter Design*) - 30 points. The symbolic state transition table for a particular counter is shown below. Use it to answer the following questions.

PS	NS	Output $Z_2 Z_1 Z_0$
S_a	S_b	000
S_b	S_c	011
S_c	S_d	101
S_d	S_e	111
S_e	S_a	100
S_f	S_a	001
S_g	S_a	010
S_h	S_a	110

- a. Fill in the encoded state transition table for the counter. For state assignment, encode each state with the same value as the output of that particular state. For example, since the output is 000 whenever the counter is in the state S_a , then use 000 as the state assignment for the state S_a .

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PS			NS			Output		
A	B	C	A^+	B^+	C^+	Z_2	Z_1	Z_0
0	0	0	0	1	1	0	0	0
0	1	1	1	0	1	0	1	1
1	0	1	1	1	1	1	0	1
1	1	1	1	0	0	1	1	1
1	0	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1
0	1	0	0	0	0	0	1	0
1	1	0	0	0	0	1	1	0

- b. Fill in the excitation table for the counter as we have selected J-K flip-flops to build this counter.

PS			NS						Output		
A	B	C	J_A	K_A	J_B	K_B	J_C	K_C	Z_2	Z_1	Z_0
0	0	0	0	X	1	X	1	X	0	0	0
0	1	1	1	X	X	1	X	0	0	1	1
1	0	1	X	0	1	X	X	0	1	0	1
1	1	1	X	0	X	1	X	1	1	1	1
1	0	0	X	1	0	X	0	X	1	0	0
0	0	1	0	X	0	X	X	1	0	0	1
0	1	0	0	X	X	1	0	X	0	1	0
1	1	0	X	1	X	1	0	X	1	1	0

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- c. Use KMAPs to find the minimized sum of products form for the combinational logic outputs J_A , J_B , J_C , K_A , K_B , and K_C . For example,

$$\begin{aligned}Z_2 &= A \\Z_1 &= B \\Z_0 &= C\end{aligned}$$

For J_A , we have the following groups in the KMAP: (3,7).

$$\begin{aligned}J_A &= \sum m(3) + \sum d(4, 5, 6, 7) \\&= BC\end{aligned}$$

For K_A , we have the following groups in the KMAP: (0,2,4,6).

$$\begin{aligned}K_A &= \sum m(4, 6) + \sum d(0, 1, 2, 3) \\&= \overline{C}\end{aligned}$$

c. Continued.

For J_B , we have the following groups in the KMAP: (0,2),(5,7).

$$\begin{aligned} J_B &= \sum m(0, 5) + \sum d(2, 3, 6, 7) \\ &= \overline{A} \overline{C} + AC \end{aligned}$$

For K_B , we have the following groups in the KMAP: (0,1,2,3,4,5,6,7).

$$\begin{aligned} K_B &= \sum m(2, 3, 6, 7) + \sum d(0, 1, 4, 5) \\ &= 1 \end{aligned}$$

For J_C , we have the following groups in the KMAP: (0,1).

$$\begin{aligned} J_C &= \sum m(0) + \sum d(1, 3, 5, 7) \\ &= \overline{A} \overline{B} \end{aligned}$$

For K_C , we have the following groups in the KMAP: (0,1),(6,7).

$$\begin{aligned} K_C &= \sum m(1, 7) + \sum d(0, 2, 4, 6) \\ &= \overline{A} \overline{B} + AB \end{aligned}$$

4. (*Hazard-Free Design - 20 points.*) Develop the Boolean expression in SOP form found by removing the static-one hazards from the following expression. Each gate introduced in the hazard-free circuit should have the smallest number of inputs possible. In other words, your solution should be minimized. Draw the schematic for the hazard-free circuit. Assume that literals and their complement are available as inputs.

$$F(W, X, Y, Z) = \prod M(0, 1, 2, 3, 4, 6, 12, 14)$$

Solution:

$$\begin{aligned} F(W, X, Y, Z) &= \prod M(0, 1, 2, 3, 4, 6, 12, 14) \\ &= \sum m(5, 7, 8, 9, 10, 11, 13, 15) \end{aligned}$$

For $F(W, X, Y, Z)$ we have the following groups in the KMAP: (5,7,13,15), (8,9,10,11).

$$F(W, X, Y, Z) = W \overline{X} + XZ$$

For $F_{HF}(W, X, Y, Z)$ we add the following group in the KMAP: (9,11,13,15).

$$F_{HF}(W, X, Y, Z) = W \overline{X} + XZ + WZ$$

The resulting hazard free circuit is shown in the following figure.

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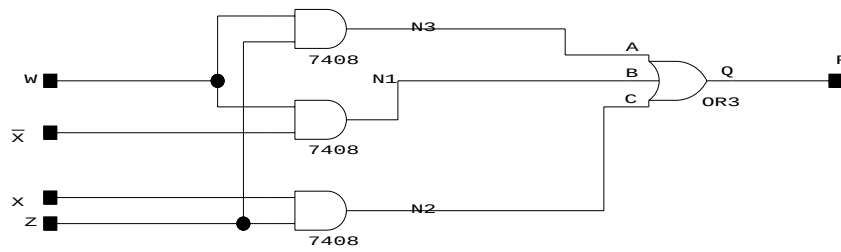


Figure 3: Figure for Problem 2.

5. (*State Assignment - 10 points.*) Given the state diagram shown in Figure Ex9.7 on page 490 in the text, select a good state assignment, justifying your answer in terms of the state assignment guidelines.

State	Assignment		
	Y_2	Y_1	Y_0
A	0	0	0
B	1	1	1
C	0	1	0
D	0	1	1
E	1	1	0

Solution:

Using the guideline for state assignment, we obtain the following constraints. High Priority: (B,C), (B,E), (C,E), (A,C), (C,D), (A,E), (B,D), (D,E). Since the number of high priority constraints is large, we need not look for medium and low priority constraints. We make the above state assignment attempting to meet as many of the constraints as possible. The following constraints were met: (B,E), (C,E), (A,C), (C,D), (B,D), (D,E)